REMARKS

I. Formal Matters. Claims 1-20 are currently pending in this application. Applicant thanks the Examiner for returning an initialled Form PTO/SB/08 A&B to signify consideration of the references submitted via the Information Disclosure Statement on March 3, 2004. In addition, Applicant thanks the Examiner for acknowledging the claim to priority under 35 U.S.C. §119 and for confirming receipt of the priority document.

II. Claims. Currently amended claims 14, 15, 19 and 20 are asserted as complying with 35 U.S.C. §101 by setting forth a proper step in a proper method claim.

Independent claim 1 is rejected as allegedly being anticipated by *Iwamoto et al.* (U.S. Patent No. 5,592,434) (*"Iwamoto"*) under 35 U.S.C. §102(b). Because the reference numbers (under the alleged §102(b) anticipation by *Iwamoto*) applied by the Examiner against Applicant's claim 1 are not accurate, Applicant begins by addressing this discrepancy. The Examiner cites Fig. 1, and references numbers 1aa, 2aa, 4aa, and 3aa as corresponding to a memory cell, a row address decoder, a column decoder, and a sense amplifier, respectively (OA page 3-4). In turn, Applicant refers to Figs. 1 and 19 with corresponding text at col. 14, line 66 to col. 15, line 14 and col. 1, line 32 to col. 3, line 50, respectively (*Iwamoto*). Therein, Applicant finds that reference numbers 1a in Fig. 1 and 51a in Fig. 19 identify a two-dimensional memory array. Further, reference numbers 52a, 53a and 54a identify a row address decoder, a column decoder, and a sense amplifier, respectively.

Next, the Examiner asserts that reference number 9aa of Fig. 1 identifies a clock storage section (OA page 4). However, neither in Figs. 1 and 19, nor in the text at large, does *Iwamoto* disclose a clock storage section for storing of external clock data. Reference number 59a of Figs. 1 and 19 identifies a write register (*Iwamoto,* col. 2, lines 22-30). The write register stores write data, not clock data, received from input buffer 58a.

However, *Iwamoto* does disclose using an external clock. Specifically, *Iwamoto* discloses taking in externally applied control signals in synchronization with an external clock (circuit 62) to generate a first set of internal control signals (*Iwamoto,* col. 3, lines 10-20; Fig 19, ref. 62). Subsequently, a second set of control signals are generated (circuit 63) in response to the first set of internal control signals and a clock counter 64 (*Iwamoto,* col. 3, lines 20-30; Fig. 19). This second set of internal control signals includes a sense amplifier activation signal.

While claim 1 is rejected as being allegedly anticipated by *Iwamoto* under 35 U.S.C. §102(b), the Examiner applies "*Sato*" (U.S. Patent No. 5,892,730) (OA page 2). *Sato* contains the reference numbers 1aa, 2aa, 4aa and 3aa, which correspond to a memory array, a row address decoder, a column decoder, and a sense amplifier, respectively. Similar to *Iwamoto, Sato* discloses a write register 9aa (*Sato,* Fig. 1). Selector 8a first stores internal write data in write register 9aa; data D0, applied in the first clock cycle, is stored in register 9aa. Data D1 is stored at the next clock cycle in write register 9ab (*Sato,* col. 6, lines 38-44; Figs. 39-40; col. 14, lines 39-49; Fig. 1). Write data is stored in write registers at a rate determined by a clock cycle.

Further, similar to *Iwamoto*, *Sato* also discloses using an external clock. Specifically, *Sato* discloses clock input buffer 34 which receives an external clock signal (extCLK) (*Sato,* Fig. 2). Clock input buffer 34 produces a pulse signal having a predetermined time width in synchronization with rising of extCLK, and generates the same as internal clock signal CLK (*Sato,* col. 15, lines 31-37). Subsequently, a second set of control signals are generated (circuit 32) in response to the first set of internal control signals and a clock counter 17 (*Sato,* col. 15, lines 46-55; Fig 2). This second set of internal control signals includes a sense amplifier activation signal.

In contrast, Applicant claims the storage of a property of an external clock data for use in generating a sense amplifier activation signal. Specifically, Applicant claims, "a synchronous type semiconductor memory device comprising...a clock data storage section..." (claim 1). This data indicates a property, for example frequency, of the clock signal. Three or more kinds of clock data can be stored ([0055]). Further, Applicant claims generation of a sense amplifier activation signal based on the clock data and the row address strobe signal (claim 1). At least for failing to disclose the element of a clock data storage section storing clock data, where the clock data is used as a basis for sense amplifier activation signal, Applicant asserts that the rejection of claim 1 as being allegedly anticipated by *Iwamoto* under 35 U.S.C. §102(b) is improper and should be withdrawn. Likewise, at least for failing to disclose the element of a clock data storage section storing clock data, where the clock data is used as a basis for sense amplifier

activation signal, Applicant asserts that a rejection of claim 1 as being allegedly anticipated by *Sato* under 35 U.S.C. §102(b) would be improper.

Independent claim 11 is rejected as allegedly being anticipated by *Iwamoto* under 35 U.S.C. §102(b). Claim 11 also contains the element of storing clock data and generating a sense amplifier activation signal based on said clock data (claim 11). Therefore, the arguments asserted in traversal of claim 1 are hereby asserted for claim 11. At least for failing to disclose the element of storing clock data and generating a sense amplifier activation signal based on said clock data, Applicant asserts that the rejection of claim 11 as being allegedly anticipated by *Iwamoto* under 35 U.S.C. §102(b) is improper and should be withdrawn.

Dependent claims 2-7 and 12-20 are asserted as being in condition for allowance, at least for depending from an allowable independent claim.

Allowable Subject Matter. Applicant thanks the Examiner for indicating that claims 8-10 contain allowable subject matter of a sequence of delay elements for shifting of a row/column address strobe signal. Method claim 18 and amended method claims 19 and 20 also contain the Examiner-identified allowable subject matter of a sequence of delay elements for shifting of a column address strobe signal.

In view of the preceding amendments and remarks, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephonic

interview, the Examiner is kindly requested to contact the undersigned attorney at the local telephone number listed below.

The USPTO is directed and authorized to charge all required fees (except the Issue/Publication Fees) to our Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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